IN THE CLAIMS:

Please amend claim 51, and add new claims 79 through 84, all
to read as indicated below:

1   1.   (previously presented)   Apparatus for deterring failure of a
2   computing system; said apparatus comprising:
3   a hardware network of components, having substantially no
4   software and substantially no firmware except programs held in an
5   unalterable read-only memory;
6   terminals of the network for connection to such system; and
7   fabrication-preprogrammed hardware circuits of the network
8   for guarding such system from failure.

1   2.   (previously presented)   The apparatus of claim 1, particu-
2   larly for use with such system that is substantially exclusively
3   made up of commercial, off-the-shelf components; and wherein:
4   at least one of the network terminals is connected to re-
5   ceive at least one error signal generated by such system in event
6   of incipient failure of such system;
7   at least one of the network terminals is connected to pro-
8   vide at least one recovery signal to such system upon receipt of
9   the error signal; and
10   the apparatus further comprises means for automatically
11 responding to the at least one error signal by generating the at
12 least one recovery signal for guarding all of such system against
13 failure.

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1   3.   (previously presented)   The apparatus of claim 1, wherein:

2   the network is an infrastructure which is generic in that it

3   can accommodate any such system that can issue an error message

4   and handle a recovery command.

1   4.   (original)   The apparatus of claim 1, further comprising:

2   such computing system.

1   5.   (original)   The apparatus of claim 1, wherein:

2   the circuits comprise portions for identifying failure of

3   any of the circuits and correcting for the identified failure.

1   6.   (previously presented)   The apparatus of claim 1, wherein:

2   the circuits are not capable of running any application pro-

3   gram.

1   7.   (original)   The apparatus of claim 1, particularly for use

2   with a computing system that is substantially exclusively made of

3   commercial, off-the-shelf components and that has at least one

4   hardware subsystem for generating a response of the system to

5   failure; and wherein:

6   the circuits comprise portions for reacting to said response

7   of such hardware subsystem.

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1   8.   (original)   The apparatus of claim 1, particularly for use

2   with a computing system that has plural generally parallel

3   computing channels; and wherein:

4   the circuits comprise portions for comparing computational

5   results from such parallel channels.

1   9.   (previously presented)   The apparatus of claim 8, wherein:

2   the parallel channels of such computing system are of di-

3   verse design or origin.

1   10.   (original)   The apparatus of claim 1, particularly for use

2   with a computing system that has plural processors; and wherein:

3   the circuits comprise portions for identifying failure of

4   any of such processors and correcting for identified failure.

1   11.   (previously presented)   The apparatus of claim 1, wherein:

2   the circuits comprise modules for collecting and responding

3   to data received from at least one of the terminals, said modules

4   comprising:

5

6   at least three data-collecting and -responding modules,

7   and

8

9   processing sections for conferring among the modules to

10   determine whether any of the modules has failed.

1   12. (previously presented) The apparatus of claim 1, particu-
2   larly for use with a computing system that is substantially
3   exclusively made of commercial, off-the-shelf components and that
4   has at least one subsystem for generating a response of the
5   system to failure, and that also has at least one subsystem for
6   receiving recovery commands; and wherein:
7   the circuits comprise portions for interposing analysis and
8   a corrective reaction between the response-generating subsystem
9   and the command-receiving subsystem.

1   13. (previously presented) Apparatus for deterring failure of
2   an entire computing system, wherein the computing system option-
3   ally includes plural mutually redundant modules; said apparatus
4   comprising:
5   a network of components having terminals for connection to
6   such system, wherein the network is constructed to be initially
7   and permanently distinct from such computing system including all
8   of such redundant modules if present; and
9   circuits of the network for operating programs to guard such
10   entire system from failure;
11   the circuits comprising portions for identifying failure of
12   any of the circuits and correcting for the identified failure.

1   14. (previously presented) The apparatus of claim 13, wherein:
2   the program-operating portions comprise a section that
3   corrects for the identified failure by automatically taking a
4   failed circuit out of operation.

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15. (previously presented) The apparatus of claim 13, wherein:
     the network is an infrastructure that continuously waits to
respond to messages from such system.

1 16. (original) The apparatus of claim 13, further comprising:
2   such computing system.

1 17. (original) The apparatus of claim 13, wherein:
2   the program-operating portions comprise at least three of
3 the circuits; and
4   failure is identified at least in part by majority vote
5 among the at least three circuits.

1 18. (previously presented) The apparatus of claim 13, wherein:
2   said circuits receive from such system error messages warn-
3 ing of incipient failure, and issue recovery commands to such
4 system.

1 19. (previously presented) The apparatus of claim 13, particu-
2 larly for use with a computing system that is substantially
3 exclusively made of commercial, off-the-shelf components and that
4 has at least one hardware subsystem for generating a response of
5 the system to failure; and wherein:
6   the circuits comprise portions for reacting to said response
7 of such hardware subsystem.

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1 20. (original) The apparatus of claim 13, particularly for use
2 with a computing system that has plural generally parallel com-
3 puting channels; and wherein:
4   the circuits comprise portions for comparing computational
5 results from such parallel channels.

1 21. (previously presented) The apparatus of claim 16, wherein:
2   the computing system has parallel channels that are of di-
3 verse design or origin.

[FOR THE EXAMINER'S CONVENIENCE: PLEASE SEE NEW CLAIM 70,
PREFERABLY FOR INSERTION HERE.]

1 22. (original) The apparatus of claim 13, particularly for use
2 with a computing system that has plural processors; and wherein:
3   the circuits comprise portions for identifying failure of
4 any of such processors and correcting for identified failure.

1 23. (previously presented) The apparatus of claim 13, wherein:
2   the network is an infrastructure which is generic in that it
3 can accommodate any such system that can issue an error message
4 and handle a recovery command.

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1 24. (previously presented) The apparatus of claim 13, particu-

2 larly for use with a computing system that is substantially

3 exclusively made of commercial, off-the-shelf components and that

4 has at least one subsystem for generating a response of the

5 system to failure, and that also has at least one subsystem for

6 receiving recovery commands; and wherein:

7   the circuits comprise portions for interposing analysis and

8 a corrective reaction between such response-generating subsystem

9 and such command-receiving subsystem.

25. -   32. (canceled)

1 33. (previously presented) Apparatus for deterring failure of a

2 computing system that is substantially exclusively made of com-

3 mercial, off-the-shelf components and that has at least one

4 hardware subsystem for generating an error message of the system

5 about incipient failure; said apparatus comprising:

6   a network of components having terminals for connection to

7 such system; and

8   circuits of the network for operating programs to guard such

9 system from failure;

10   the circuits comprising portions for reacting to such error

11 message of such hardware subsystem.

1 34. (previously presented) The apparatus of claim 33, wherein:

2   the circuits guard the entire such system from failure.

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1　35. (previously presented) The apparatus of claim 33, wherein:

2　　　the network is generic in that it can accommodate any such

3　system that can issue an error message and handle a recovery

4　command.

1　36. (original) The apparatus of claim 33, further comprising:

2　　　such computing system, including such hardware subsystem.

1　37. (previously presented) The apparatus of claim 36, wherein:

2　　　the computing system has plural generally parallel computing

3　channels; and

4　　　the parallel channels of the computing system are of diverse

5　design or origin.

1　38. (previously presented) The apparatus of claim 33, wherein:

2　　　said circuits are not capable of operating any application

3　program.

39. and 40. (canceled)

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1 41. (previously presented) The apparatus of claim 33, particu-

2 larly for use with a computing system that is substantially

3 exclusively made of commercial, off-the-shelf components and that

4 has at least one subsystem for generating a response of the

5 system to failure, and that also has at least one subsystem for

6 receiving recovery commands; and wherein:

7   the circuits comprise portions for interposing analysis and

8 a corrective reaction between such response-generating subsystem

9 and such command-receiving subsystem.

1 42. (previously presented) Apparatus for deterring failure of

2 an entire computing system that is distinct from the apparatus

3 and that has plural generally parallel computing channels and has

4 at least one application-data input module, and at least one

5 processor for running an application program; said apparatus

6 comprising:

7   a network of components having terminals for connection to

8 such system; and

9   circuits of the network for operating programs to guard such

10 entire system from failure, wherein the network is constructed to

11 be initially and permanently distinct from such computing system

12 including substantially (a) every such application-data input

13 module and (b) every such application-program processor, and (c)

14 all of such parallel computing channels;

15   the circuits comprising portions for comparing computational

16 results from such parallel channels.

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1   43.   (original)   The apparatus of claim 47, wherein:

2   the parallel channels of the computing system are of diverse

3   design or origin.

1   44.   (original)   The apparatus of claim 42, wherein:

2   the comparing portions comprise at least one section for

3   analyzing discrepancies between the results from such parallel

4   channels.

1   45.   (previously presented)   The apparatus of claim 44, wherein:

2   the circuits are not capable of running any application pro-

3   gram.

1   46.   (currently amended)   The apparatus of claim 42, [[,]] where-

2   in:

3   the network is an infrastructure which is generic in that it

4   can accommodate any such system that can issue an error message

5   and computational results, and handle a recovery command.

1   47.   (original)   The apparatus of claim 42, further comprising:

2   such computing system.

1   48.   (previously presented)   The apparatus of claim 42, wherein:

2   the circuits do not and cannot operate any application

3   program.

EXAMINER B. P. BONZO / 09/886,959   **11**   P. LIPPMAN / xAAA-02

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1   49.   (previously presented)   The apparatus of claim 48, wherein:

2   the circuits receive from such computing system error mes-

3   sages warning of incipient failure and issue recovery commands to

4   such computing system.

1   50.   (previously presented)   Apparatus for deterring failure of a

2   computing system that is distinct from the apparatus and that has

3   plural generally parallel computing channels; said apparatus

4   comprising:

5   a network of components having terminals for connection to

6   such system; and

7   circuits of the network for operating programs to guard such

8   system from failure, wherein such network is constructed to be

9   initially and permanently distinct from such computing system in-

10 cluding all of such parallel computing channels;

11   the circuits comprising portions for comparing computational

12 results from such parallel channels; and wherein:

13   the comparing portions comprise circuitry for performing an

14 algorithm to validate a match that is inexact; and

15   the algorithm-performing circuitry employs a degree of inex-

16 actness suited to a type of computation under comparison.

1   51.   (currently amended)   The apparatus of claim 50, wherein:

2   the algorithm-performing circuitry performs an algorithm

3   that selects a degree of inexactness based on type of computation

4   under comparison; and

5   the circuits also impose corrective action upon such system

6   based upon discrepancies found by the comparing portions.

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[FOR THE EXAMINER'S CONVENIENCE: PLEASE SEE NEW CLAIM 71 THROUGH 74,

PREFERABLY FOR INSERTION HERE.]

1   52.   (original)   The apparatus of claim 42, particularly for use

2   with a computing system that has plural processors; and wherein:

3   the circuits comprise portions for identifying failure of

4   any of such processors and correcting for identified failure.

1   53.   (original)   The apparatus of claim 42, wherein:

2   the circuits comprise modules for collecting and responding

3   to data received from at least one of the terminals, said modules

4   comprising:

5

6   at least three data-collecting and -responding modules,

7   and

8

9   processing sections for conferring among the modules to

10   determine whether any of the modules has failed.

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1   54. (previously presented) The apparatus of claim 42, particu-
2   larly for use with a computing system that is substantially
3   exclusively made of commercial, off-the-shelf components and that
4   has at least one subsystem for generating a response of the
5   system to failure, and that also has at least one subsystem for
6   receiving recovery commands; and wherein:
7   the circuits comprise portions for interposing analysis and
8   a corrective reaction between such response-generating subsystem
9   and such command-receiving subsystem.

1   55. (previously presented) Apparatus for deterring failure of
2   any computing system that has plural processors and has at least
3   one application-data input module, and at least one processor for
4   running an application program, and is capable of generating an
5   error message warning of incipient failure and capable of re-
6   sponding to a recovery command; said apparatus comprising:
7   a network of components having terminals for connection to
8   such system, wherein the network is constructed to be initially
9   and permanently distinct from such any computing system including
10 substantially (a) every such application-data input module and
11 (b) every such application-program processor, and (c) all of such
12 plural processors; and
13   circuits of the network for operating programs to guard any
14 such system from failure;
15   the circuits comprising portions for identifying failure of
16 any of such processors and correcting for identified failure.

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[FOR THE EXAMINER'S CONVENIENCE: PLEASE SEE NEW CLAIM 75,

PREFERABLY FOR INSERTION HERE.]

1   56.   (previously presented)   The apparatus of claim 75, wherein:

2   the identifying portions comprise a section that corrects

3   for the identified failure by taking a failed processor out of

4   operation.

    57.   (previously presented)   The apparatus of claim 75, wherein:

          the circuits cannot and do not run an application program.

1   58.   (previously presented)   The apparatus of claim 75, wherein:

2   the circuits protect the entire such computing system.

1   59.   (previously presented)   The apparatus of claim 75, further

2   comprising:

3   such computing system.

    60.   (canceled)

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1 61. (previously presented) The apparatus of claim 75, par-

2 ticularly for use with a computing system that is substantially

3 exclusively made of commercial, off-the-shelf components and that

4 has at least one subsystem for generating a response of the

5 system to failure, and that also has at least one subsystem for

6 receiving recovery commands; and wherein:

7   the circuits comprise portions for interposing analysis and

8 a corrective reaction between such response-generating subsystem

9 and such command-receiving subsystem.

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1   62.   (previously presented)   Apparatus for deterring failure of

2   an entire computing system that is distinct from the apparatus

3   and has at least one application-data input module, and at least

4   one processor for running an application program; said apparatus

5   comprising:

6   a network of components having terminals for connection to

7   such system; and

8   circuits of the network for operating programs to guard such

9   entire system from failure;

10   the circuits comprising modules for collecting and respond-

11   ing to data received from at least one of the terminals, said

12   modules comprising:

13

14   at least three data-collecting and -responding modules,

15   and

16

17   processing sections for conferring among the modules to

18   determine whether any of the modules has failed;

19

20   wherein the network, including all of the modules and sub-

21   stantially (a) every such application-data input module and (b)

22   every such application-program processor, and (c) all of the

23   processing sections, is constructed to be initially and perma-

24   nently distinct from such computing system.

1   63.   (original)   The apparatus of claim 62, further comprising:

2   such computing system.

1 64. (original) The apparatus of claim 62, particularly for use

2 with a computing system that is substantially exclusively made of

3 commercial, off-the-shelf components and that has at least one

4 subsystem for generating a response of the system to failure, and

5 that also has at least one subsystem for receiving recovery

6 commands; and wherein:

7   the circuits comprise portions for interposing analysis and

8 a corrective reaction between such response-generating subsystem

9 and such command-receiving subsystem.

[FOR THE EXAMINER'S CONVENIENCE: PLEASE SEE NEW CLAIMS 76 THROUGH 78,

PREFERABLY FOR INSERTION HERE.]

1 65. (previously presented) Apparatus for deterring failure of a

2 computing system that is substantially exclusively made of com-

3 mercial, off-the-shelf components and that has at least one

4 subsystem for generating a response of the system to failure, and

5 that also has at least one subsystem for receiving recovery

6 commands; said apparatus comprising:

7   a network of components having terminals for connection to

8 such system between the response-generating subsystem and the

9 recovery-command-receiving subsystem; and

10   circuits of the network for operating programs to guard such

11 system from failure;

12   the circuits comprising portions for interposing analysis

13 and a corrective reaction between the response-generating sub-

14 system and the command-receiving subsystem.

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1   66.   (previously presented)   The apparatus of claim 65, further

2   comprising:

3   such computing system.

1   67.   (previously presented)   The apparatus of claim 65, wherein:

2   the circuits cannot and do not run any application program.

1   68.   (previously presented)   The apparatus of claim 65, wherein:

2   the circuits protect the entire such system.

1   69.   (previously presented)   The apparatus of claim 65, wherein:

2   the network is an infrastructure which is generic in that it

3   can accommodate any such system that can issue an error message

4   and handle a recovery command.

1   70.   (previously presented)   The apparatus of claim 13, wherein:

2   the circuits do not and cannot operate any application pro-

3   gram.

1   71.   (previously presented)   The apparatus of claim 50, wherein:

2   the circuits cannot and do not run any application program.

1   72.   (previously presented)   The apparatus of claim 50, wherein:

2   the circuits protect the entire such system.

1 73. (previously presented) The apparatus of claim 50, wherein:

2   the circuits receive from such computing system error messa-

3 ges warning of incipient failure and issue recovery commands to

4 such computing system.

1 74. (previously presented) The apparatus of claim 50, wherein:

2   the network is an infrastructure which is generic in that it

3 can accommodate any such system that can issue an error message

4 and computational results, and can handle a recovery command.

1 75. (previously presented) The apparatus of claim 55, wherein:

2   the program-operating circuits guard any such system from

3 failure by issuing a recovery command; and

4   the failure-identifying and correcting portions provide the

5 recovery command.

1 76. (previously presented) The apparatus of claim 62, wherein:

2   the circuits cannot and do not run any application program.

1 77. (previously presented) The apparatus of claim 62, wherein:

2   the circuits protect the entire such system.

1 78. (previously presented) The apparatus of claim 62, wherein:

2   the network is an infrastructure which is generic in that it

3 can accommodate any such system that can issue an error message

4 and handle a recovery command.

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1   79.   (new)   The apparatus of claim 1, wherein:

2   the apparatus is not a circuit breaker.

1   80.   (new)   The apparatus of claim 1, wherein:

2   at least one of the network terminals is connected to re-

3   ceive at least one error signal generated by such system in event

4   of incipient failure of such system;

5   at least one of the network terminals is connected to pro-

6   vide at least one recovery signal to such system upon receipt of

7   the error signal.

1   81.   (new)   An infrastructure for a computing system that has

2   at least one computing node ("C-node") for running at least one

3   application program; said infrastructure comprising:

4   at least one monitoring node ("M-node") for monitoring the

5   condition of the at least one C-node by waiting for an error sig-

6   nal, indicating incipient failure, from the at least one C-node

7   and responding to the error signal by sending a recovery command

8   to the at least one C-node; and

9   at least one adapter node ("A-node") for transmitting the

10 error signal and recovery command between the at least one C-node

11 and at least one M-node; and wherein:

12   the at least one M-node is manufactured, and remains, wholly

13 distinct from the at least one C-node; and

14   the at least one M-node cannot, and does not, run any appli-

15 cation program.

1   82.   (new)   The infrastructure of claim 81, further comprising:

2   such computing system.

1   83.   (new)   The infrastructure of claim 81, particularly for use

2   with such computing system that has plural such C-nodes; and

3   further comprising:

4   a decision-making node ("D-node") for comparing output data

5   generated by such plural C-nodes and reporting to the at least

6   one M-node any discrepancy between the output data; and wherein:

7   the at least one M-node analyzes the D-node reporting, and

8   based thereon arbitrates among the C-nodes.

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1   84.   (new)   The infrastructure of claim 81, further comprising:

2   at least one self-checking node for startup, shutdown and

3   survival ("S3-node"), specifically for executing power-on and

4   power-off sequences for such system and for the infrastructure,

5   and for receiving error signals and sending recovery commands to

6   the at least one M-node.

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